Amendments to the Specification:

[0008] FIGs. 14-17, Kimura shows forming a first gate oxide film 1a having a first portion on one side of a field oxide 2 and a second portion on an opposite side of the field oxide. The first portion of the first gate oxide is masked with photoresist (PR) ~~105a~~. Wet etching removes the second portion of first gate oxide. Then the photoresist is stripped, and thermal oxidation is performed again. This forms a new, second gate oxide in the second portion, and increases the thickness of the remaining first portion of the first gate oxide. Kimura recognizes that photoresist in contact with the first gate oxide is not desirable, since is contains impurities. Kimura also recognizes that precleaning prior to growing the second gate oxide will also undesirably etch the first gate oxide.

[0009] In FIGs. 18-23, Kimura shows forming a first gate oxide film 1a having a first portion on one side of a field oxide ~~2~~ and a second portion on an opposite side of the field oxide. A first polycrystalline silicon film ~~204a~~ doped with an impurity is formed on the entire surface, as a protective film for the first gate oxide film 1a. The first portion of the first gate oxide is masked with photoresist (PR) ~~105a~~. Then, the polysilicon over the second portion of the gate oxide is etched away. ~~Them~~ Then, the photoresist is stripped, and thermal oxidation is performed again. This forms a new, second gate oxide in the second portion, and forms an oxide coating ~~6~~ on the polysilicon over the first ~~poriton~~ portion of the first gate oxide. In this embodiment, the entrance of Na impurities from the photoresist into the first gate oxide is prevented. Therefore, the first gate oxide film 1a is prevented from being rendered conductive, and variation of the threshold voltage of the MOS transistor is prevented.